RCY

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,050	12/29/2000	Ravi Subramanian	9824-035-999	8994

24341 7590 06/24/2004

MORGAN, LEWIS & BOCKIUS, LLP.
3300 HILLVIEW AVENUE
PALO ALTO, CA 94304

EXAMINER	
BURD, KEVIN MICHAEL	
ART UNIT	**PAPER NUMBER**
2631	

DATE MAILED: 06/24/2004

10

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,050	SUBRAMANIAN ET AL.	
	Examiner	Art Unit	
	Kevin M Burd	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This office action, in response to the amendment filed 3/31/2004, is a final office action.

Response to Arguments

2. Applicant's arguments filed 3/31/2004 have been fully considered but they are not persuasive. Applicant states there is virtually no disclosure in Dao as to what is included in its hardware accelerator and there is no disclosure or suggestion in Dao that the hardware accelerator included a plurality of computation units. The examiner disagrees. Dao states the hardware accelerator comprises a memory (column 2, lines 4-5), means for controlling direct memory transfers to move data across bus 112 (column 2, lines 5-6), additional memories (column 2, lines 13-19), additional busses (column 2, lines 13-19) and interfaces between the hardware accelerator and the DSP (column 2, lines 13-19). All of these elements are computation units. In addition, the hardware accelerator performs the processing steps that the DSP 108 is too inefficient to perform (column 2, lines 1-3). Examples of computationally intensive tasks are various coding and compression algorithms, filtering operations and data transforms (column 1, lines 29-32). Dao further discloses the use of numerous hardware accelerators as shown in figure 2. Dao states a plurality of memories will be used (column 2, lines 13-19). These memories will be homogeneous computation units. Dao also discloses the computation units comprise memories, busses and interfaces (column 2, lines 13-19). These computation units are heterogeneous. Applicant states

claim 9 is specifically directed to a base station transceiver. In response to applicant's arguments, the recitation a base station transceiver has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

For these reasons and the reasons stated in the previous office action, the rejections of the claims are maintained. Rejections of the newly added claims are found below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-12, 14, 15, 17, 18, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dao et al (US 6,275,891) in view of Lowe et al (US 6,173,243).

Regarding claims 1, 6, 9 and 10, Dao discloses the signal processing apparatus in figure 1. This circuitry is modified to provide an additional hardware accelerator (channel pooling signal processor) to carry out specific algorithms (column 1, lines 61-

63). The hardware accelerator is coupled to the DSP 109 (column 1, lines 64-66) and the DSP performs less computationally intensive tasks than the hardware accelerator (column 1, line 66 to column 2, line 3). The hardware accelerator includes its own memory buffer and directs the transfer of data over the bus 112 (column 2, lines 4-6). This data transfer is the managing of data flow into and out of the channel pooling signal processor. Since the hardware accelerator comprises a hardware accelerator for quickly carrying out specific algorithms and a memory buffer, it comprises a plurality of computational units.

Dao does not disclose a test interface for testing the function of the plurality of computation units. Lowe discloses it is important to provide means for testing the proper functionality of the system and to provide fault corrections during system operations (column 1, lines 19-32). It would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the testing method and components of Lowe in the apparatus of Dao. This will increase the reliability and efficiency of any computer system by minimizing or preventing the occurrences of faulty operations (column 1, lines 19-22).

Regarding claims 2 and 7, Dao discloses specific algorithms are carried out (a data sequencer for controlling program execution), a memory buffer (dedicated memory) and configurable logic (the hardware accelerator is digital circuitry) in column 1, line 61 to column 2, line 13.

Regarding claims 3-5 and 8, the combination is capable of receiving multiple data streams as shown in figure 2 of Dao.

Regarding claims 11, 12, 14, 15, 17, 18, 20 and 21, Dao discloses the computation unites of the hardware accelerator will carry out computationally intensive tasks (column 2, lines 1-3). Examples of these tasks are various coding and compression algorithms, filtering operations and data transforms (column 1, lines 29-32).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 13, 16, 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dao et al (US 6,275,891) in view of Lowe et al (US 6,173,243) further in view of Stilp (US 6,097,336).

Regarding claims 13, 16, 19 and 22, the combination of Dao and Lowe discloses the signal processing apparatus and method of using the signal processing apparatus stated above in paragraph 3. The combination does not disclose what type of signals the apparatus receives. Stilp discloses a receiver for supporting numerous protocols such as TDMA and CDMA (column 18, lines 10-28). "There is significant cost advantage to supporting multiple protocols within a single system." (column 18, lines 10-28). For this reason, it would have been obvious for one of ordinary skill in the art at the

time of the invention to incorporate the teachings of Stilp into the signal processing apparatus of the combination of Dao and Lowe.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for formal communications; please mark "EXPEDITED PROCEDURE" or for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA. Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Burd, whose telephone number is (703) 308-7034. The Examiner can normally be reached on Monday-Thursday from 9:00 AM - 6:00 PM.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3800.

Kevin M. Burd
PATENT EXAMINER
6/22/2004